

# **Catastrophic Heavy-Ion Failure of a Commercial ASIC**

**By**

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**Sponsor: NASA Code AE under NASA Microelectronics Space Radiation Effects  
Program (MSREP)**

**Outline**

**I. Background**

**II. Problem**

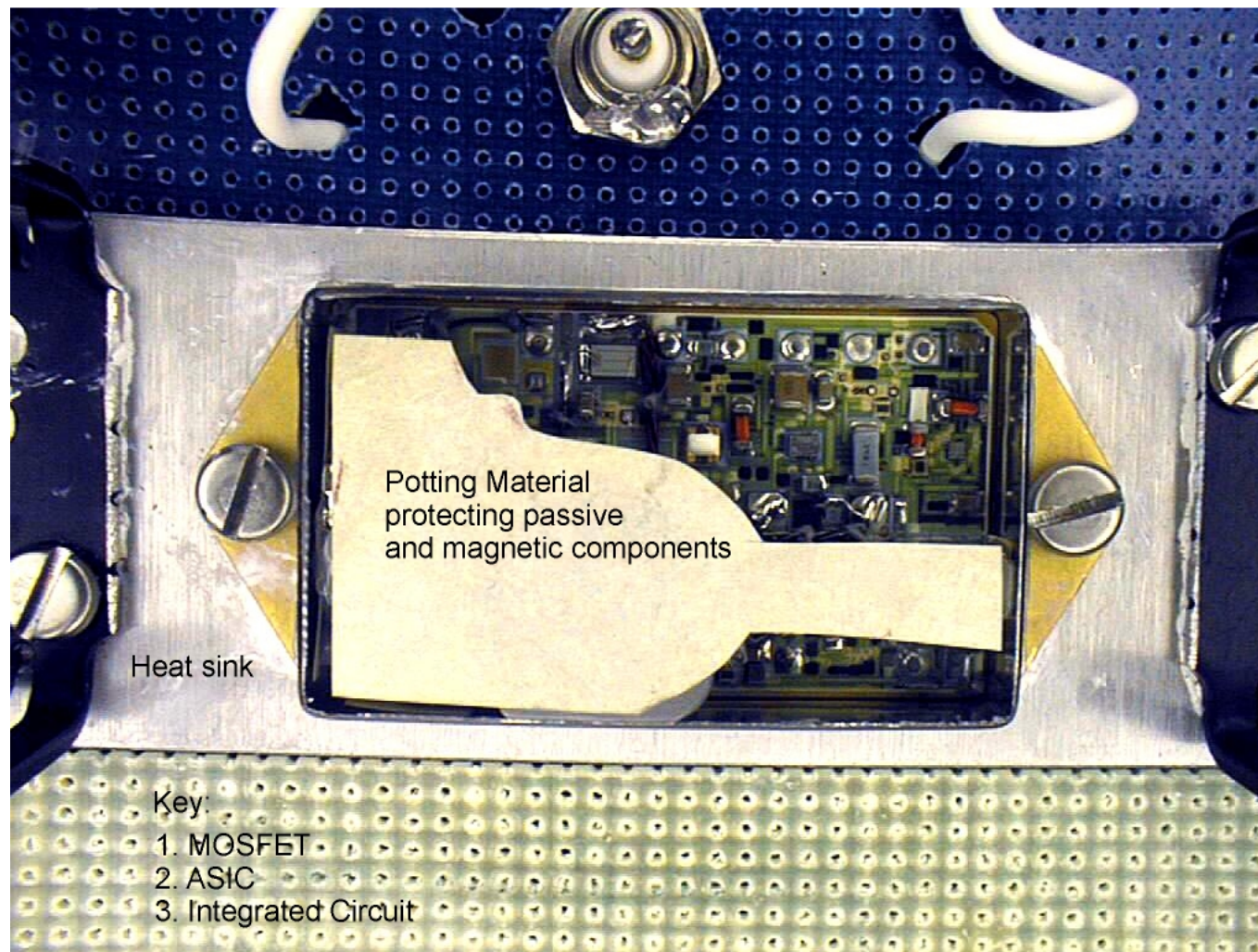
**III. Module Level Test**

**IV. Analysis**

**V. Results of radiation test**

**VI. Conclusions**

**Purpose: To Show that SEGR Occurs At Operational Voltage!**



**Multi-Chip Module mounted on test board**

## **I. Background (commercial unit)**

### **Multi-Chip Module (MCM)**

**Previous test good up to an LET < 100 MeV cm<sup>2</sup>/mg**

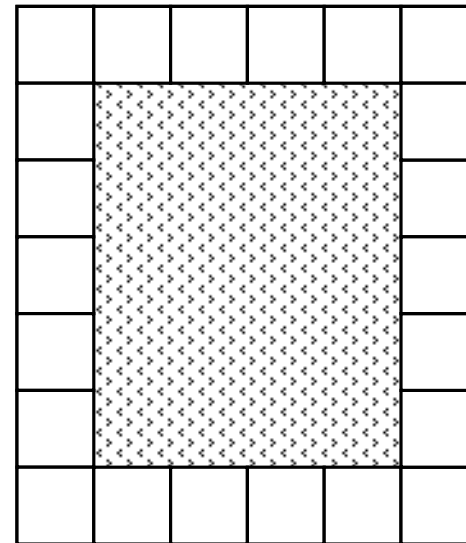
**Application Specific Integrated Circuit (ASIC) is implemented**

**By the “Sea of Transistors”**

**Around periphery**

**Drivers**

**Buffer Transistors**



**ASIC is implemented as top layer of metal**

## **II. Catastrophic Problem Low LET(BNL and Texas A&M)**

**Single-Event Latchup (SEL)?**

**Single-Event Gate Rupture (SEGR)?**

## **III. Module Level Test (SEL setup strip chart)**

**Complexity: System vs. Isolated part**

**Ideal: Statistics w/o destruction**

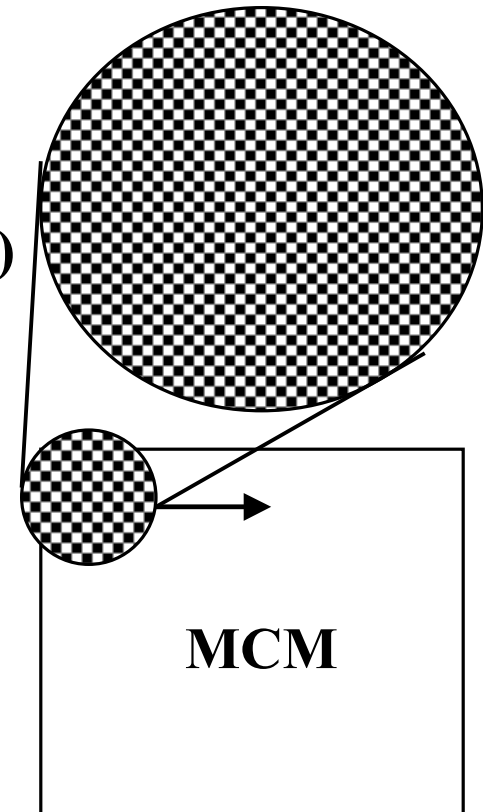
**Identifying the Culprit device**

**Small beam (Cause and effect)**

**Result: Commercial ASIC!**

**Discover: Change of Foundry (Layout same)**

**Electrical Characteristics: NEW =OLD (Not Rad.!)**



## **IV. Revisiting test result**

**Not SEGR**

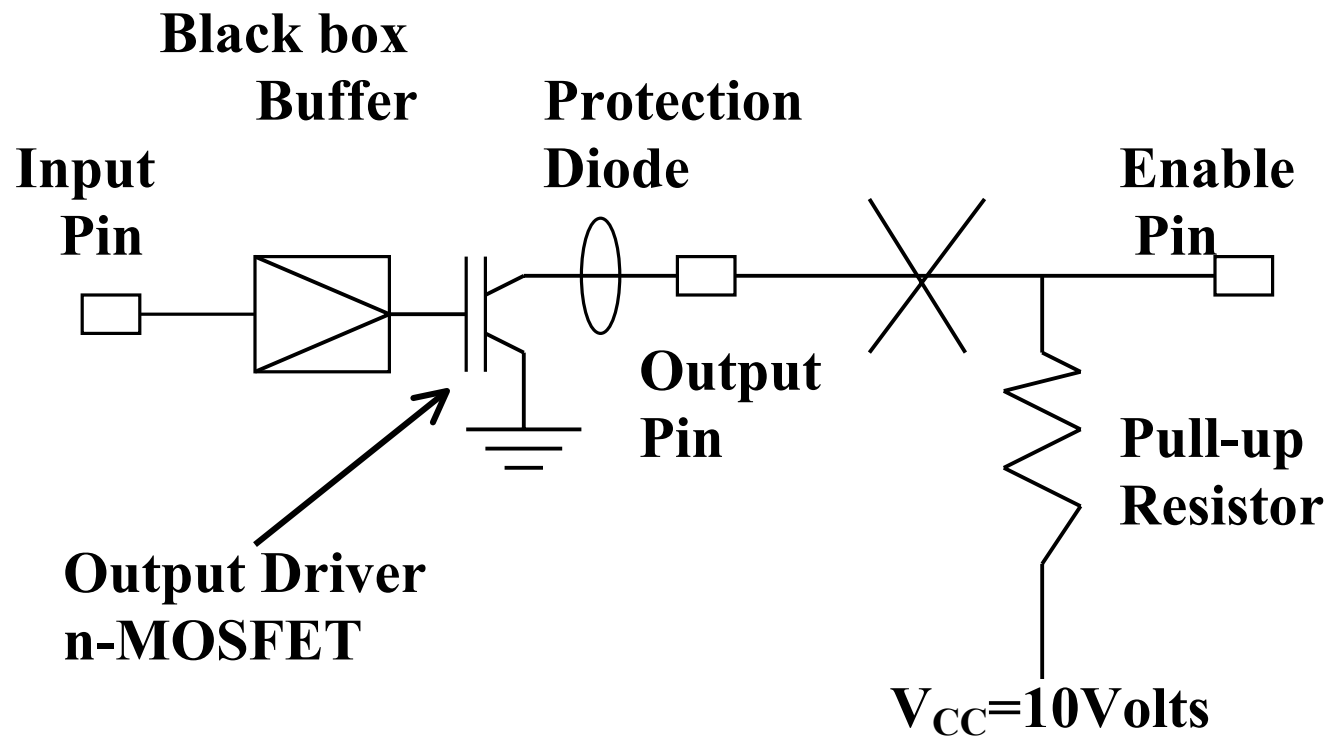
**Electric Field low ( $\sim 0.8\text{MV/cm}$ , Power MOSFET  $\sim 8\text{MV/cm}$ )**

**Not SEL**

**Unable to capture Current Signature**

- 1. Complexity**
- 2. Lack of visibility of ind. Components**
- 3. Disconnecting Enable pin      MCM Functional!**

## **“The Smoking Gun”**



**Concluded:**

- 1) Not a Latchup (cut = MCM functional)**
- 2) Isolated Transistor      SEGR experiment**

## **V. Investigated SEGR as mode of failure**

**Test ASIC alone**

**Use Californium (inc. LET 40 – 45 MeV cm<sup>2</sup>/mg)**

**Increase Voltage (SEGR is sensitive to voltage): 30V rated**

**Protection Diode (needed to prevent forward bias)**

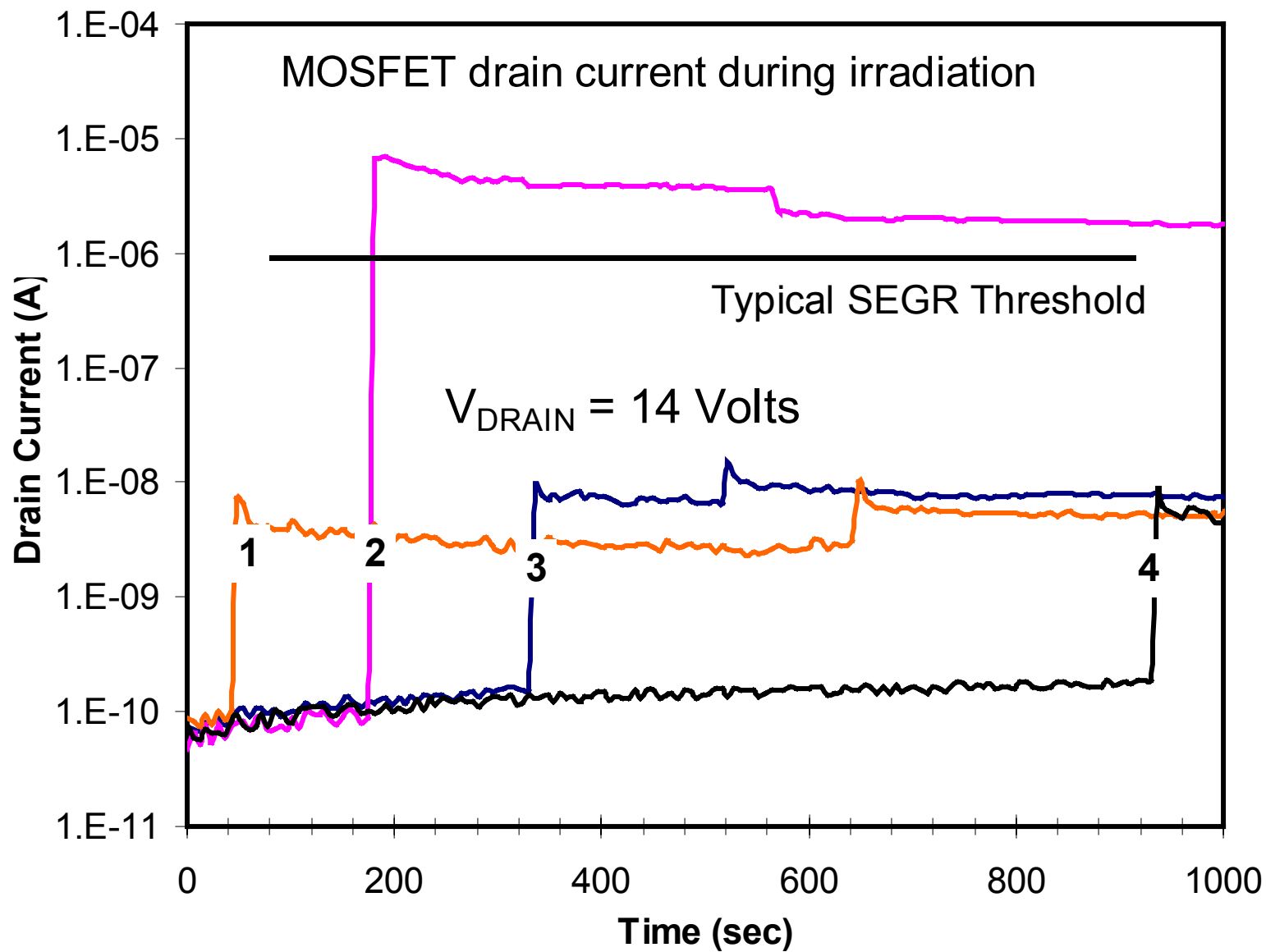
### **Methodology**

**Static Bias Condition**

**Voltage Steps (0.25 V)**

**Number of Ions ( $1 \times 10^5$ ) for 30 minutes**





## **VI. Conclusions**

- **Shown that SEGR is the failure mode for the ASIC**

**Why are there not more MOSFET failures?  
Is there a Contradiction?**

**No! “Sea of Transistors” there are SEGRs, albeit small ruptures, perhaps not enough to completely “turn on” Output MOSFET Drivers, but never-the-less gate ruptures!**

- **Question: Why SEGR at Low Voltage (14V) and Low Electric Field (0.8MV/cm) in a commercial device?**  
**This is 1 order of magnitude below Pwr MOSFETs.**
- **Is this an isolated case?**
- **Or is this the tip of an Iceberg?**

## Monologue

### Title Slide

- **My name is Luis Selva**
- **And the title of my paper is “Catastrophic Heavy-Ion Failure of a Commercial ASIC”**
- **The co-author in this paper is Gary Swift**

### Slide 2

- **The outline for this presentation is as follows;**
- **We will talk about background and a brief history of the device.**
- **Then we’ll talk about the Catastrophic problem,**
- **The Module level test,**
- **Analysis of test results,**
- **Then we’ll talk about the radiation test results**
- **And lastly we’ll draw conclusions**
- **Purpose: Show SEGR does occur in commercial devices**

**Slide 3**

- **This is a picture of the Module.**
- **The module is mounted on a heat sink**
- **The white is Potting material which is protecting passive and magnetic components underneath it.**
- **Key features of the device are the active components:**
  - 1) MOSFET**
  - 2) Integrated Circuit**
  - 3) ASIC**
  - 4) There are other active components ...**

**Slide 4**

- **Background:** We irradiated a commercial unit
- **A Multi-Chip Module (MCM),**
- **We had previously tested and was good up to LET<100**
- **Inside of the this MCM unit is an Application Specific Integrated Circuit or ASIC, which is a CMOS Gate Array**
- **For pedagogical purposes I've included this picture**
- **Around the periphery of the ASIC you'll find**
  - Drivers**
  - Buffer Transistors**
  - And in the center of the ASIC, is the “Sea of Transistors”**
  - Where all transistors are identical**
- **The ASIC application is implemented by the top metal layer**

**Slide 5**

- **The Catastrophic Problem:**

**We irradiated the MCM at Brookhaven National Laboratory and at Texas A & M.**

- **We discovered that the unit was failing catastrophically**

**Following irradiation with heavy-ions**

- **We were unable to determine the mode of failure:**

**1. Single-Event Latchup (SEL)?**

**2. Single-Event Gate Rupture (SEGR)?**

- **In order to answer this question we had to conduct a Module Level Test (System Level Test)**

- **In this experiment we setup a SEL test where we monitored currents via a stripe chart**

- **The difficulty with this experiment was getting good statistics without destroying the device**

**Module Level Test (continued)**

- **Complexities of a Module level Test:**
  - 1) **Lack of visibility into cause and effect**
  - 2) **Isolation of individual component**
- **In order to identify the culprit device, we had to reduce the beam size**
- **We swept the beam across the Multi-Chip Module**
- **We discovered that it was the Commercial ASIC that was the culprit!**
- **After this result we approached the manufacturer and inquired if there had been any design changes to the ASIC. They said “no” but added that they had change foundry!**
- **In fact, everything on the ASIC was the same including the Layout.**
- **Electrically, the pre-foundry and post-foundry changes were identical. The only difference was the Radiation Response!**

**Slide 6**

- **Based on this discussion we decided to revisit the radiation test results, in order to rule out SEL or SEGR.**
- **Reasons why it was not SEGR**
  1. **The electric field was too low  $\sim 0.8\text{MV/cm}$**   
**Typically in power MOSFETs  $E_{\text{crit}} \sim 8\text{MV/cm}$**
  2. **By disconnecting the Enable pin the Module Worked!**
- **Reasons why it was not SEL**
  1. **Unable to capture SEL signature in stripe chart**
    - a. **Were events too fast to capture? (Unlikely)**
  2. **Complexity of Module level test**
  3. **Lack of visibility into current monitoring of individual electrical components**
  4. **Disconnecting Enable Pin      module began to work following heavy-ion irradiation!**



**Slide 7****“The Smoking Gun”**

- **The gate of the Output Driver (N-MOSFET) controlled by the this Buffer (see diagram)**
- **When MOSFET “on” current flows from source to drain**
- **Protection diode**
  - A) **If forward bias current flows to  $V_{CC}$**
  - B) **If reversed bias current flows to output pin**
- **Current from output pin goes through a “pull-up” resistor and Enable pin**
- **1) Cutting the connection between output pin and the “pull-up” resistor and the MCM unit became operational not a destructive Latchup**
- **2) Disconnecting the Enable pin allowed us the ability to isolate the Output Driver (n-MOSFET) the opportunity to conduct a SEGR experiment**

**Slide 8**

- **We decided to investigate if SEGR was the failure mode**
- **In order to do this we had to test the ASIC alone**
- **We used Californium Fission fragments, LET range of 40 to 45 MEV cm<sup>2</sup>/mg**
- **We increased the drain voltage on the MOSFET by 0.25V and in some cases by 0.5V increments**
- **In order to conduct this experiment we had to prevent the protection diode from being forward bias, we could not allow the drain voltage to increase above  $V_{CC}$**
- **In order to circumvent this problem we increase  $V_{CC}$  along with the drain voltage. The offset was 0.25V.**
- **Methodology used was the standard SEGR test:**
  - **The Device was statically bias**
  - **Voltage increments between irradiation was 0.25V**
  - **Number of ions used were  $1 \times 10^5$  for 30 minute runs**

**Slide 9**

- **This graph shows the result of four radiation experiments.**
- **On the Ordinate you have Drain current in amperes**
- **And on the Abscissa you have time of exposure in seconds**
- **In a typical SEGR experiment, the current threshold for defining Gate Rupture is  $1 \times 10^{-6}$  Amps.**
- **Note that devices 1, 3, and 4 did not reach the typical SEGR threshold current. However, these are Gate ruptures, albeit small ruptures!**
- **Note that for devices 1 and 3 there are two SEGR events!**
- **These additional events are recorded because we were able to monitored the drain current (in situ) during irradiation**
- **In most SEGR experiments, SEGR classification is done post irradiation. If  $I_{\text{Drain}} \geq 1 \times 10^{-6} \text{ A}$  then SEGR.**
- **So, events that occurred in device 1 and 3 would not be classified as SEGR, typically.**

**Slide 10****• In Conclusion**

- 1. We have shown that the Catastrophic problem experienced by the ASIC is a SEGR failure mode.
  - a. Why are there not more MOSFETs failing? Is there a contradiction?**
  - b. No! Because in the “Sea of Transistors” we found SEGR, albeit small ruptures, which allowed ASIC to retain its functionality.****
- 2. Question: Why is SEGR taking place at low applied Electric Fields?**
- 3. Is this the tip of an iceberg?**
- 4. Are there other commercial devices that are sensitive heavy-ion irradiation within normal operating conditions?**

**Thank you**